

SEMINAR ANNOUNCEMENT

Quantifying the Reliability Impact of Stockpile Aging: Stress Voiding of IC Interconnects

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Abstract

The seminar presents the results of research into the statistical characterization of the aging of integrated circuit interconnect lines. The current effort extends research into the deterministic life characterization to account for uncertainties in grain size, storage temperature, void spacing and initial residual stress and their impact on interconnect failure after wafer processing. The sensitivity of the life estimates to these uncertainties is also investigated. Various methods for characterizing the probability of failure of a conductor line were investigated including: Latin hypercube sampling (LHS), quasi-Monte Carlo sampling (qMC), as well as various analytical techniques. Preliminary results indicate that the reliability of integrated circuits due to stress voiding is very sensitive to the underlying uncertainties associated with grain size and void spacing. In particular, accurate characterization of IC reliability depends heavily on not only the first and second moments of the uncertainty distribution, but more specifically the unique form of the underlying distribution. *A particularly interesting result of this research is the demonstration that high quality control during wafer processing can have a significant, negative impact on the storage reliability of integrated circuits. Similarly, a 'dirty', out-of-control manufacturing process can lead to a more reliable component.*